Amendments to the Specification:

Please replace the last paragraph of page 6 (lines 5-20) of the Specification with the following paragraph.

Fig. 1B shows an example of four pixels 100 binned together by electrical connections 102 to form a combined pixel 110. Fig. 1C shows the cross section view of the part of an imager shown in Fig. 1A showing an example of a programmable electrical connection used to bin pixels together. In this example, shown in Fig. 1C, a first N^- well 12 and a second N^- well are formed in a P^- type substrate 10. A N^+ region 22 is formed in the P^- substrate 10 between the first N^- well 12 and the second N^- well 14. A gate oxide 24 is formed over the N^+ region 22 and a gate electrode 26 is formed over the gate oxide 24. The first N^- well 12, the N^+ region 22, and the second N^- well 14 then form an N channel FET which can be turned on or off to either bin the two pixels together or to isolate the two pixels. This binning method allows programmable binning of selected pixels so that the resolution can be changed by programming signals to the imager. The resolution of the imager can be changed within a frame or between frames as desired. This binning method is explained in Patent Application Serial No. 10/339,189, entitled "APS PIXEL WITH RESET NOISE SUPRESSION AND PROGRAMMABLE BINNING CAPABILITY" by Taner Dosluoglu, Filed January 9, 2003 which is now U.S. Patent Number 6,878,918 B2 and is incorporated herein by reference.